CHRISTOPHER
VEGA

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EDUCATION

Bachelor of Science | Florida International University
RECEIVED FALL 2018

Master of Science | University of Florida
RECEIVED SPRING 2022

Doctor of Philosophy| University of Florida
EXPECTED SUMMER 2023

SKILLS AND TECHNOLOGIES

Programming Languages: C, C++, Java, Python, Verilog, VHDL

Tools: Cadence, AutoCAD, Altium Designer, Atmel Studio, Multisim, MatLab, Quartus, Vivado, Git, Splunk, Jira, Jenkins, Fortify, Mockito

Skills: Circuit Design and Analysis, Microprocessor programming, Embedded systems design, FPGA design, Sensors, Electrochemical impedance spectroscopy, JTAG programming/debugging

RESEARCH INTERESTS

- Hardware Security and Trust
- Embedded Systems Design
- Cyber Security

PROJECTS

Automatic Implementation of Secure Silicon (AISS)

Development of a secure automated System on Chip (SoC) design that scales security measures with the chip design. AISS aims to address four specific attacks, side channel attacks, reverse engineering attacks, supply chain attacks, and malicious hardware attacks. I primarily worked on integrating a PUF for system authentication into the secure security engine design.

SPLIT FPGA PUF

An FPGA based PUF which repurposes existing elements to reduce PUF overhead. Targeting the 6-input look-up table (LUT) architecture present on Xilinx devices the LUT be split in half. The functional logic can occupy one half with the other half utilized as a PUF. This allows for the PUF to be embedded alongside and spread throughout the functional logic.

Memory in Logic PUF

A synthesizable physical unclonable function (PUF) designed for use on FPGAs. Through judicious selection of circuit gates, existing circuit elements can be repurposed to function as a PUF. This allows for the PUF to be distributed throughout the FPGA device.

JTAG IOLock

Modification of the JTAG architecture allowing for encryption of data being sent over I/O pins. The modification allows for transmission encryption keys over secure methods allowing for obfuscation of IC functionality.

EMPLOYMENT HISTORY

Hardware Security Research Intern, | MIT Lincoln Laboratory
SEPTEMBER 2022 – DECEMBER 2022

Performed research involving FPGA PUF, which could reutilize existing reconfigurable elements on the device for reduced overhead. A LUT-level netlist was generated for a design. Half-utilized LUTs were selected and combined with our PUF architecture. Alongside the PUF architecture, a set of tools was developed to insert the PUF into designs and apply FPGA design constraints. Experiments were conducted to analyze PUF performance and stability under a range of different temperatures.

Cyber Security Research Intern, | Los Alamos National Laboratory
JUNE 2021 – AUGUST 2022

Performed cyber security research that involved designing, developing, and analyzing Physical Unclonable Functions (PUFs). My main responsibilities involved the implementation and analysis of a machine-learning attack on different PUF solutions. Additionally, assisted with the implementation of a PUF hardware solution as well as analyzing the quality and security metrics of the collected data.

Software Engineer Intern/Junior Dev, | First Data
MAY 2018 – JUNE 2019

Development, deployment, and maintenance of RESTful web services for use in Visa and Master Card credit card transactions. Web services were programmed in Java in a test for development style. Along with development, security audits of current using Fortify tools were also performed. Audits aimed to solve log injection issues, prevent leaking sensitive information, ensure proper encryption was used, ect.

RESEARCH EXPERIENCE

Pre-Doctoral Fellow/Research Assistant, | University of Florida
AUGUST 2019 - CURRENT

Graduate Research in the Warren B. Nelms Institute under Dr. Bhunia. Research focuses on Hardware Security and Internet of Things with projects relating to Trojan detection, design validation, IP protection, and logic locking. Also involved in projects relating to the design of self-aware systems, machine learning, electric vehicle charging and implantable/wearable devices.

Undergraduate Research Assistant, | Florida International University
JANUARY 2018 – JUNE 2019

Undergraduate research assistant in the Bio Sensors lab under Dr. Mubarak. Research focuses on automating electrochemical impedance spectroscopy measurements through a multi-electrode device to detect abnormalities in live cells such as cancer.

PUBLICATIONS

- C. Vega, S. Deb Paul, P. SLPSK, A. Chatterjee, S. Bhunia, "MeLPUF: Memory-in-Logic PUF Structures for Low-Overhead IC Authentication" (Under Review)
- C. Vega, P. SLPSK, S. Bhunia, "IOLock: An Input/Output Locking Scheme for Chip and PCB Protection against Reverse-Engineering Attacks" (In Preparation)
- C. Vega, "Resource-efficient PUF Implementation Through FPGA Resource Re-utilization" (In Submission)

CONFERENCE POSTER PRESENTATIONS

- C. Vega, P. SLPSK, S. Bhunia, "FPGA Security Solutions through SRAM based PUFs", DAC, 2020, Virtual
- (Presented on Behalf of) A. Dasgupta, M. Rahman, N. Dorairaj, D. Kehlet, S. Bhunia, "RIPPER: Securing Hardware IP through Fine Grained Redaction of Boolean Functions", GOMACTech, 2022, Miami, FL
- C. Vega, P. SLPSK, S. Bhunia, "IOLock: An Input/Output Locking Scheme for Chip and PCB Protection", GOMACTech, 2023, San Diego, CA (Upcoming)
- C. Vega, S. Deb Paul, P. SLPSK, S. Bhunia, "MeLPUF: Memory-in-Logic PUF Structures for Low-Overhead IC Authentication", Florida Semiconductor Week, 2023, Gainesville, FL

PATENTS

- C. Vega, R. Dizon-Paradis, S. Deb Paul, P. Difuntorum, S. Bhunia, "DJIN: Defense of JTAG I/O Network" (Published)
- C. Vega, S. Deb Paul, S. Bhunia, "Memory in Logic Physical Unclonable Function" (Published)
- C. Vega, R. Dizon-Paradis, P. SLPSK, R. Reddy, S. Bhunia, "Reconfigurable JTAG Architecture for Implementation of Programmable Hardware Security Features in Digital Designs" (Filed)
- R. Dizon-Paradis, P. Chakraborty, P. SLPSK, C. Vega, P. Difuntorum, S. Bhunia, "Drone-based Administration of Remotely Located Instruments and Gadgets" (Published)
- C. Vega, P. SLPSK, S. Bhunia, "FPGA PUF Authentication Scheme" (ongoing)